microwave JOURNAL®

New Synthesis and Simulation Software to Enhance the Design Process

How much automation are current electronic design automation (EDA) tools providing? While the RF computer aided engineering (CAE) industry has a lot to offer in the way of automated circuit and system analysis, what about automated circuit synthesis? The circuit design project that starts with one of the typical simulation programs on the market today probably isn't benefited by design automation as much as it could be. The reason for this is that many of these software programs are simulation focused rather than design focused. In other words, these programs can do a good job of analyzing or even optimizing an existing circuit design, but do little or nothing to aid the engineer in coming up with the circuit topology in the first place. The result is that the design engineer is forced into a kind of backward process of trial and error in developing an initial circuit design or prototype. Moreover, when only simulation and optimization are employed, the design process can fail completely.

Some simulation programs attempt to assist the designer by providing example schematics of common circuits. However, there is no guarantee that the circuit topology provided will satisfy a new set of specifications, even after employing optimization. Consider, for example, the output matching network for an RF amplifier. One of the most economical circuits for narrow-band matching is the two-element L network. There are eight different ways an inductor or capacitor can be combined to form an L network. At least one of these L networks is capable of matching any (real or complex) source to any other (real or complex) load. While there may be several L configurations that will provide a match, not all eight will work for a given source and load impedance. Therefore, if one of these L configurations is borrowed from an existing de-

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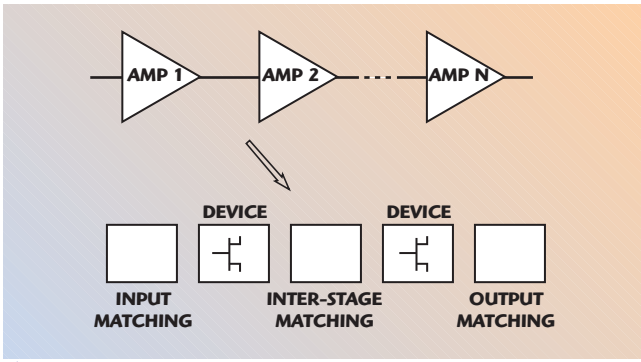

Fig. 1 A multi-transistor amplifier cascade.

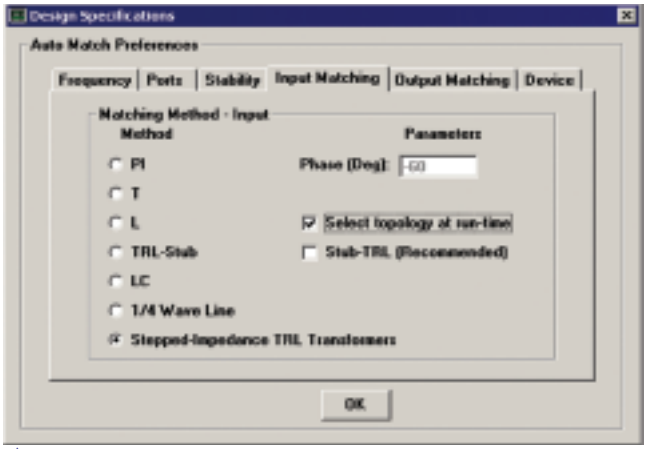

Fig. 2 The Design Specifications form opened to the Input Matching menu.

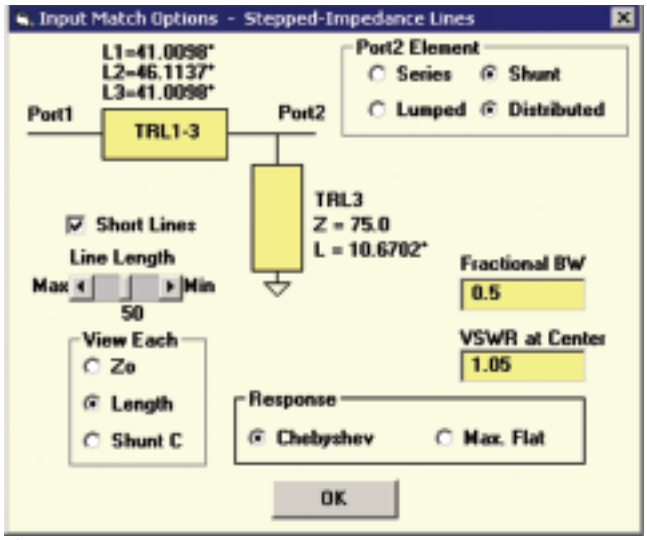

Fig. 3 Input matching options for stepped-impedance lines.

sign and applied to a new device or load it is likely to fail to provide an impedance match, even after lengthy attempts to use an optimizer. The designer may not realize the futility of the attempt until a great deal of time has been expended.

The optimizer in the simulation program fails because it cannot know beforehand which topology will solve the problem. In contrast, a circuit synthesis program can select the correct topology and provide the exact component values.

Another situation in which the optimizer is sure to fail is when the goal is to provide a conjugate match to both ports of a potentially unstable device. A simultaneous bilateral conjugate match is not possible unless the potentially unstable device is first rendered unconditionally stable at the design (match) frequency. Resistive loading at the input or output terminals of the device or various forms of feedback can usually stabilize the device. However, neither the simulator nor the optimizer is equipped to alter the circuit topology appropriately.

A new software package created by Dale Henkes of ACS (Applied Computational Sciences, Escondido, CA) and available from Artech House Inc. solves these problems by combining circuit synthesis, schematic capture and simulation into a powerful integrated design environment. The program's name, FAST: Fast Amplifier Synthesis Tool, refers not only to the speed at which new designs are turned into circuit schematics (and verified through simulation), but also to how quick and easy it is to use the tool. With a built-in parts library of more than 40 circuit elements and schematic symbols, the schematic capture and simulation portions of the program could be used as a powerful stand-alone circuit simulator. Circuit schematics can be manually created and analyzed as in any general-purpose circuit simulator. However, the main focus of the program is its ability to automatically synthesis single- and multi-stage RF and microwave amplifier circuits, complete with input matching, output matching and any inter-stage matching networks. The program can turn a simple specification form for a multi-transistor amplifier cascade, as shown in ***Figure 1***, into a circuit schematic with a single menu click. After filling in a specifications form, the entire process, from circuit synthesis through performance analysis and verification, can be accomplished in just three clicks — click Design, click Analyze and click View Results.

The designer customizes the design using the Design Specifications form. Some of the characteristics that can be controlled are the design frequency, port impedances, stability, input and output matching methods, and the type and number of devices used in the design. ***Figure 2*** shows this form opened to the Input Matching tab. A large variety of lumped and distributed network topologies are immediately available for selection. However, there are many more network variations available than first meets the eye. In fact the number of variations on most of the major network categories are essentially unlimited.

For example, the phase shift through the PI and T networks can be specified. This generates a new three-element matching network for any given phase angle. This gives the designer control over the circuit Q, type of components used (inductor or capacitor) and the part's value.

Another category providing unlimited variations is the Stepped-Impedance TRL Transformers matching method. If the default version of this method is selected, then the program will automatically employ conventional quarter-wave stepped-impedance transmission line transformers for the matching network.

The user, however, can gain access to a great deal of detailed control over the circuit by choosing to select the topology at run-time (during synthesis). As shown in ***Figure 3***, some of these specifications include control over the bandwidth, the in-band VSWR, the line lengths, the type of element used to cancel the reactance at port 2 (the

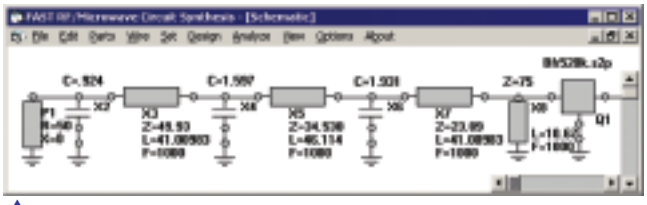

Fig. 4 Synthesis results for the stepped-impedance line example.

device or load end), whether the element is lumped or distributed, placed in shunt or series orientation, and, if distributed, the characteristic impedance of the line. The frequency response of the network can also be shaped by selecting Chebyshev or maximally flat functions.

The ability to control the line length (for what would otherwise be a series of fixed-length quarter-wave lines) adds important new design flexibility. Consider, for example, a three-section microstrip stepped-impedance transformer designed for 1000 MHz using a 32-mil substrate having a dielectric constant of 3.38. Each quarter-wave line would be approximately 1.8" long for a total length of 5.4". In order to accommodate the physical constraints of limited circuit board real estate or smaller packaging, the designer may resort to using material with a higher dielectric constant. This new FAST short line method allows for continuous adjustment of all line lengths down to a fraction of their original quarter-wave length. This is accomplished while maintaining the impedance match at the design frequency and without the need to increase the substrate's dielectric constant. Of course the substrate's dielectric constant could also be increased for further compacting.

Another benefit of using the short line method occurs from the addition of shunt capacitors placed at the junctions of the series transmission lines, as shown in ***Figure 4***. Adjustment of the values of these capacitors can facilitate tuning of the physical prototype on the bench.

Figure 4 shows the synthesis results for the input matching options specified in Figure 3. Three transmission lines (approximately one-eighth wavelength long), three shunt capacitors and a 75 Ω shorted stub at the input terminal of the device make up the input network. A circuit simulation, resulting in a detailed performance analysis, can be conducted using these electrical models, or the transmission line models can first be converted to microstrip or stripline.

All of the transmission line elements in the schematic can be automatically converted to microstrip or stripline (physical dimensions of length and width) by selecting Convert T-Lines to Microstrip/Stripline from the Design menu. ***Figure 5*** shows the results of a two-stage amplifier synthesized by FAST and converted to microstrip. Smith chart plots of S_{11} and S_{22} indicate a near perfect match at the design frequency, while the graph reports a gain of more than 32 dB.

FAST provides exceptional design flexibility while maintaining simple user control over the entire process. For example, the schematic shows that an inter-stage matching network matches the output of the first device (the BFR520K transistor) directly to the input of the second device (the NE02135 transistor). The Design Specifications form provides a list of inter-stage matching choic-

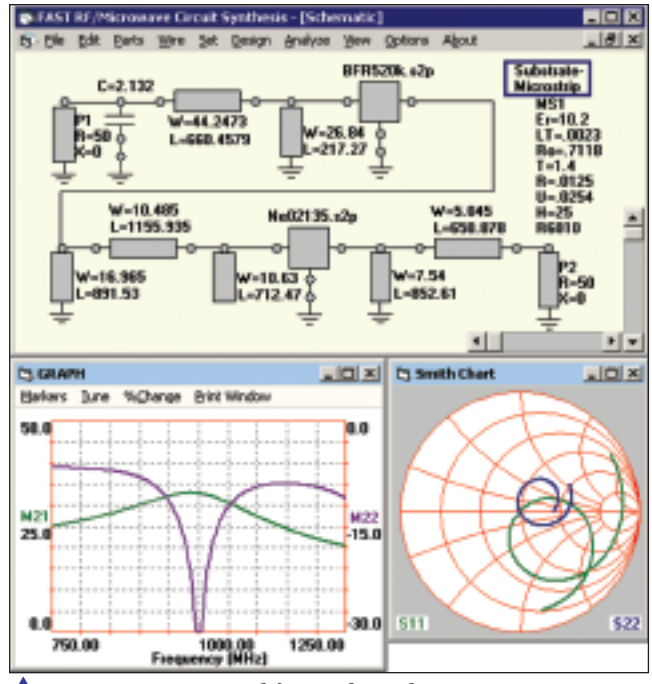

Fig. 5 A two-stage amplifier synthesized using FAST.

es that will provide this direct match. More importantly, perhaps, the program allows the user to design an inter-stage network that will match to any intermediate impedance level before matching to the next device. The later option constructs an insertion point between the stages where a device, such as a filter, can be placed without disturbing the circuit. The inter-stage impedance level can be set to any value so that the design can accommodate an inter-stage signal conditioning device or filter of any impedance value.

Even if an inter-stage filter is not needed, it is sometimes useful to design a 50 Ω point between stages to accommodate the connection of test equipment.

In addition to automated multi-stage amplifier design and simulation, FAST includes a unique low noise amplifier (LNA) design suite. This comprehensive set of tools includes all of the gain, noise, stability and matching information needed to evaluate the suitability of an LNA device to meet the design requirements. Moreover, the LNA design tool provides a number of automated design guides and strategies for a more tailored implementation. These include available power gain, operating power gain, maximum available gain (MAG), minimum noise figure and a unique control for trading off available gain for noise performance. Gain and noise trade-offs can be made visually and interactively by simply moving a slider control toward maximum gain or minimum noise. Displayed gain and noise circles respond instantly to show the best match point on a Smith chart while readouts of noise figure and associated gain are continuously updated. At any point a complete amplifier schematic can be generated that captures the current design strategy and performance requirements.

All of the FAST matching methods for amplifier design are also available separately for solving general impedance matching problems. Clicking Design/Match generates a matching network schematic using the impedance data

and network type from the Design Specifications form. If two port symbols (source and load) are placed on a blank schematic window, then selecting Match from the Design menu will automatically build a matching network connecting the two ports. The ports can be edited to specify any impedance (real or complex).

CONCLUSION

The new FAST RF circuit design and simulation program has been described. This time-saving software offers invaluable assistance in the following areas:

- Fast direct circuit synthesis and simulation
- Automatic matching network synthesis
- Automatic schematic conversion to stripline or microstrip from ideal transmission line models
- Single-stage or multi-stage amplifier design
- Flexible design control and inter-stage matching choices
- Automatic device stabilization
- Expert application of low noise design techniques
- Gain and noise figure trade-off analysis
- Gain and stability trade-off analysis
- Tuning and manual editing of schematics
- Monte Carlo statistical yield analysis

This unique design tool automates complex RF and microwave circuit development, reducing design work to a fast and efficient three-step process. Each step requires only a single mouse click to complete. Click Design and the circuit design is automatically captured on a schematic page. Click Analyze and a circuit simulator generates a detailed performance analysis.

Click View Results and the displayed results can be printed or saved to disk for later editing and further analysis. The circuit can be saved as a schematic or the simulation can be exported to other programs as an S-parameter file.

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